

Digital Systems Testing Testable Design

Digital Systems Testing and Testable Design Digital System Test and Testable Design Power-Constrained Testing of VLSI Circuits Digital Systems Testing And Testable Design Digital Systems Testing & Testable Design Encyclopedia of Microcomputers Tutorial--VLSI Testing & Validation Techniques Encyclopedia of Computer Science and Technology Techniques for Design and Testing of Iterative and Systolic Arrays Design and Testing of Regular Circuits International Workshop on Electronic Design, Test and Applications VLSI Fault Modeling and Testing Techniques IEEE VLSI Test Symposium Testing's Impact on Design & Technology VLSI System Test Records of the 1993 IEEE International Workshop on Memory Testing, August 9-10, 1993, San Jose, California Mathematical Design Proceedings Records of the 1995 IEEE International Workshop on Memory Technology, Design, and Testing, August 7-8, 1995, San Jose, California Test-driven Transformations in Logic Design Miron Abramovici Zainalabedin Navabi Nicola Nicolici Miron Abramovici Miron Abramovici Allen Kent Hassan K. Reghbaty Allen Kent Hasan Eli Elhuni Ronald DeShawn Blanton Michel Renovell George W. Zobrist Rochit Rajsuman J. Paul Roth Rochit Rajsuman Michael James Batek

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Testing Techniques IEEE VLSI Test Symposium Testing's Impact on Design & Technology
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1995, San Jose, California Test-driven Transformations in Logic Design *Miron Abramovici*
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this updated printing of the leading text and reference in digital systems testing and testable design provides comprehensive state of the art coverage of the field included are extensive discussions of test generation fault modeling for classic and new technologies simulation fault simulation design for testability built in self test and diagnosis complete with numerous problems this book is a must have for test engineers asic and system designers and cad developers and advanced engineering students will find this book an invaluable tool to keep current with recent changes in the field

this book is about digital system testing and testable design the concepts of testing and testability are treated together with digital design practices and methodologies the book uses verilog models and testbenches for implementing and explaining fault simulation and test generation algorithms extensive use of verilog and verilog pli for test applications is what distinguishes this book from other test and testability books verilog eliminates ambiguities in test algorithms and bist and dft hardware architectures and it clearly describes the architecture of the testability hardware and its test sessions describing many of the on chip decompression algorithms in verilog helps to evaluate these algorithms in terms of hardware overhead and

timing and thus feasibility of using them for system on chip designs extensive use of testbenches and testbench development techniques is another unique feature of this book using pli in developing testbenches and virtual testers provides a powerful programming tool interfaced with hardware described in verilog this mixed hardware software environment facilitates description of complex test programs and test strategies

this text focuses on techniques for minimizing power dissipation during test application at logic and register transfer levels of abstraction of the vlsi design flow it surveys existing techniques and presents several test automation techniques for reducing power in scan based sequential circuits and bist data paths

this textbook provides a comprehensive and detailed treatment of digital systems testing and testable design it covers thoroughly both the fundamental concepts and the latest advances in this rapidly changing field and presents only theoretical material that supports practical applications successfully used worldwide this book is an invaluable tool for test engineers asic and system designers and cad developers

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the encyclopedia of microcomputers serves as the ideal companion reference to the popular encyclopedia of computer science and technology now in its 10th year of publication this timely reference work details the broad spectrum of microcomputer technology including

microcomputer history explains and illustrates the use of microcomputers throughout academe business government and society in general and assesses the future impact of this rapidly changing technology

case based reasoning to user interface software tools

a collection of the 78 oral presentations and 24 poster papers from the january 2002 international workshop which brought together specialists from a broad area of electronic design manufacturing test and advanced system applications in the hope that the conference would integrate design test and application as cross dependent disciplines the contributions are organized into sessions focusing on analog test communications digital signal processing and architectures low to high level fault simulation and identification high level design memory power issues in design and test sensor and analog design electrical engineering education electromagnetics and control fault tolerant digital systems image processing robotics submicron technology test generation and compaction and test techniques and methodologies annotation copyrighted by book news inc portland or

vlsi systems are becoming very complex and difficult to test traditional stuck at fault problems may be inadequate to model possible manufacturing defects in the integrated circuit hierarchical models are needed that are easy to use at the transistor and functional levels stuck open faults present severe testing problems in cmos circuits to overcome testing problems testable designs are utilized bridging faults are important due to the shrinking geometry of ics bist pla schemes have common features controllability and observability which are enhanced through additional logic and test points certain circuit topologies are more easily testable than others the amount of reconvergent fan out is a critical factor in determining realistic measures for

determining test generation difficulty test implementation is usually left until after the vlsi data path has been synthesized into a structural description this leads to investigation methodologies for performing design synthesis with test incorporation these topics and more are discussed

from the august 1993 workshop in san jose california 26 papers report the latest findings on testing computer memory the sections include test pattern generation algorithms fault models testing for process defects and yield improvement and radiation issues and space applications no subject i

electrical engineering computer science mathematical design building reliable complex computer systems ieee press series on engineering of complex computer systems phillip a laplante and alexander d stoyen series editors as computer technology advances the debugging process for complex computer systems has become increasingly difficult to meet the challenge of program verification computer engineers are turning to mathematical techniques in hardware design brought to you by distinguished scholar j paul roth mathematical design offers key insights into the research and development of the design of computers and computer systems this book features authoritative coverage of the most important topics in the field two level logic minimization verification of a supercomputer the ibm 3081 algorithm for ac dynamic testing diagnosis demonstration of hardware and software equivalence complete with thought provoking exercises and engaging commentary mathematical design is an excellent reference for practicing hardware designers as well as other engineers with an interest in computer science and mathematics

this annual workshop serves as a forum for the exchange of ideas on semiconductor

memories design and testing the proceedings of the 1995 workshop include a tutorial session testing random access memories and 18 papers in six technical sessions role of simulation in memory design bridging fault

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